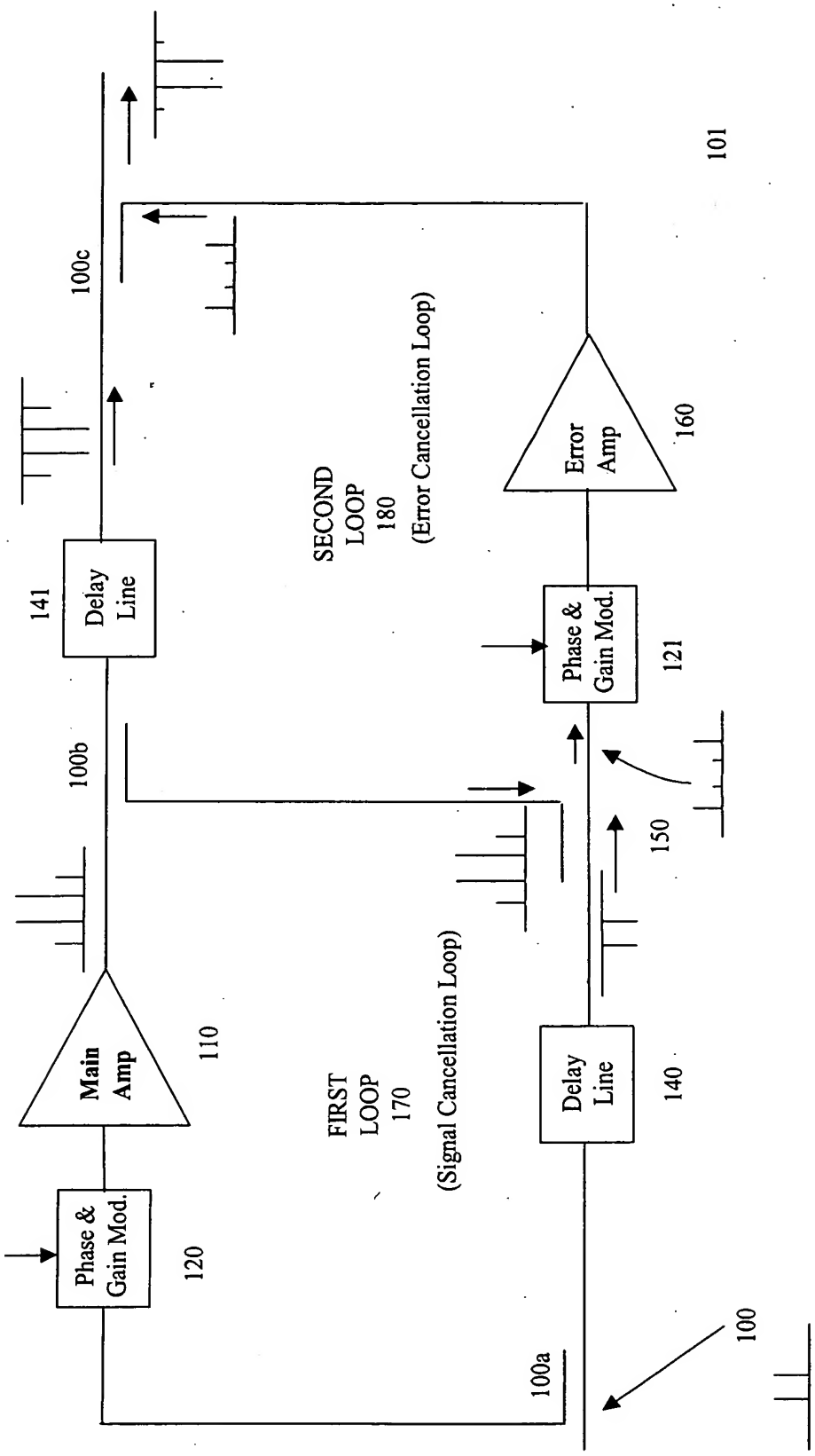


PRIOR ART

FIG. 1

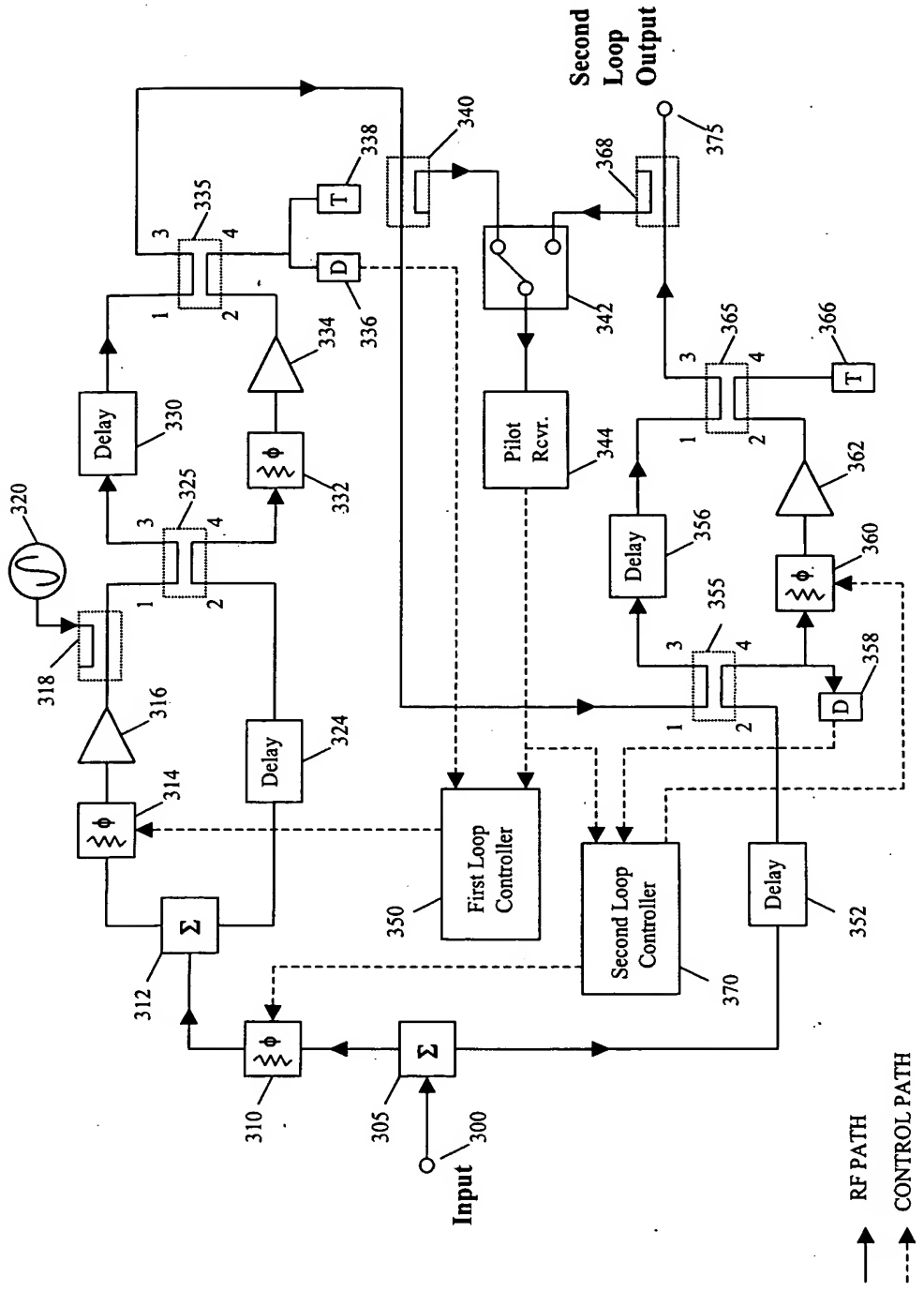


FIG. 2

PRIOR ART

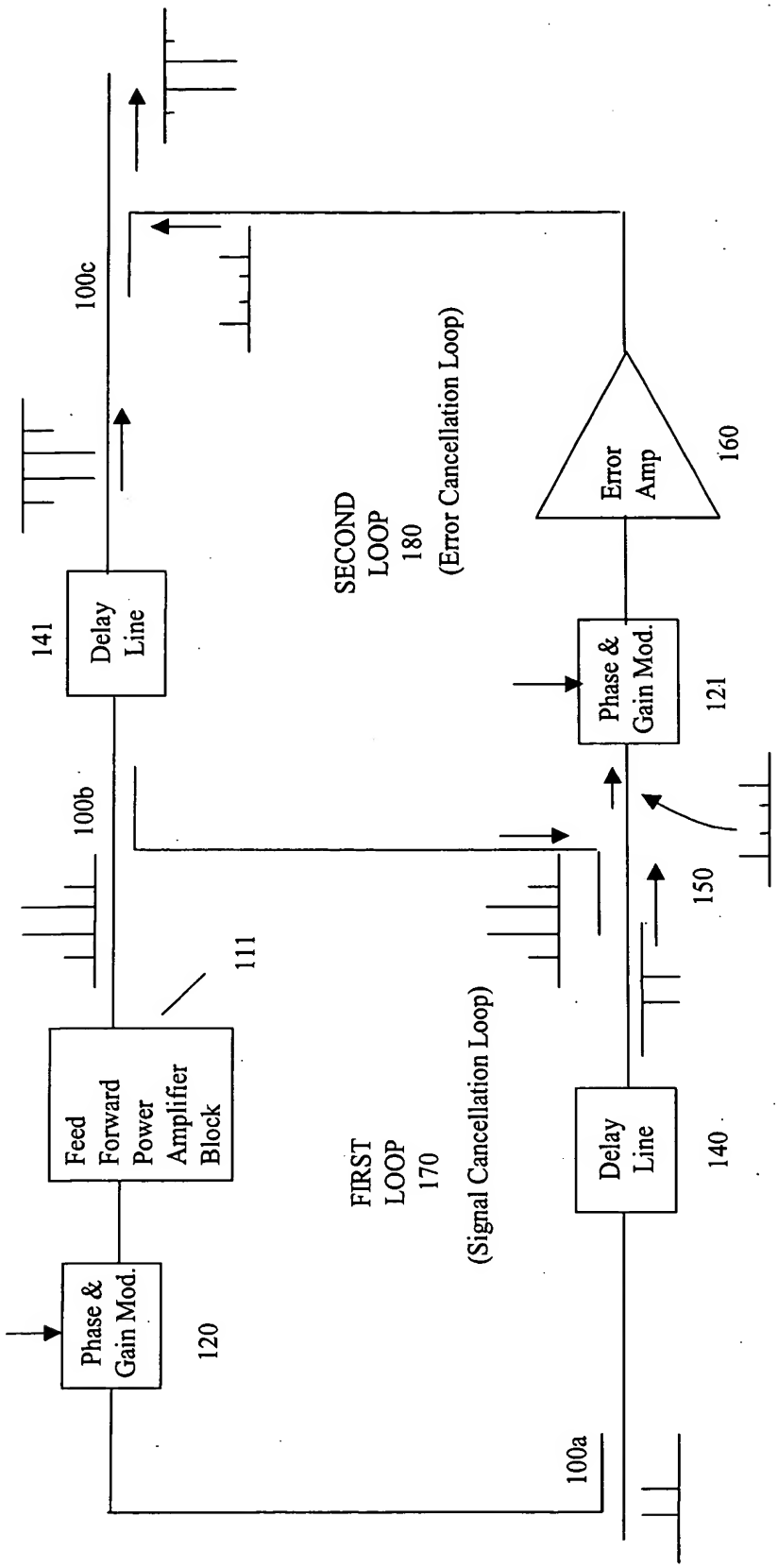


FIG. 3

PRIOR ART

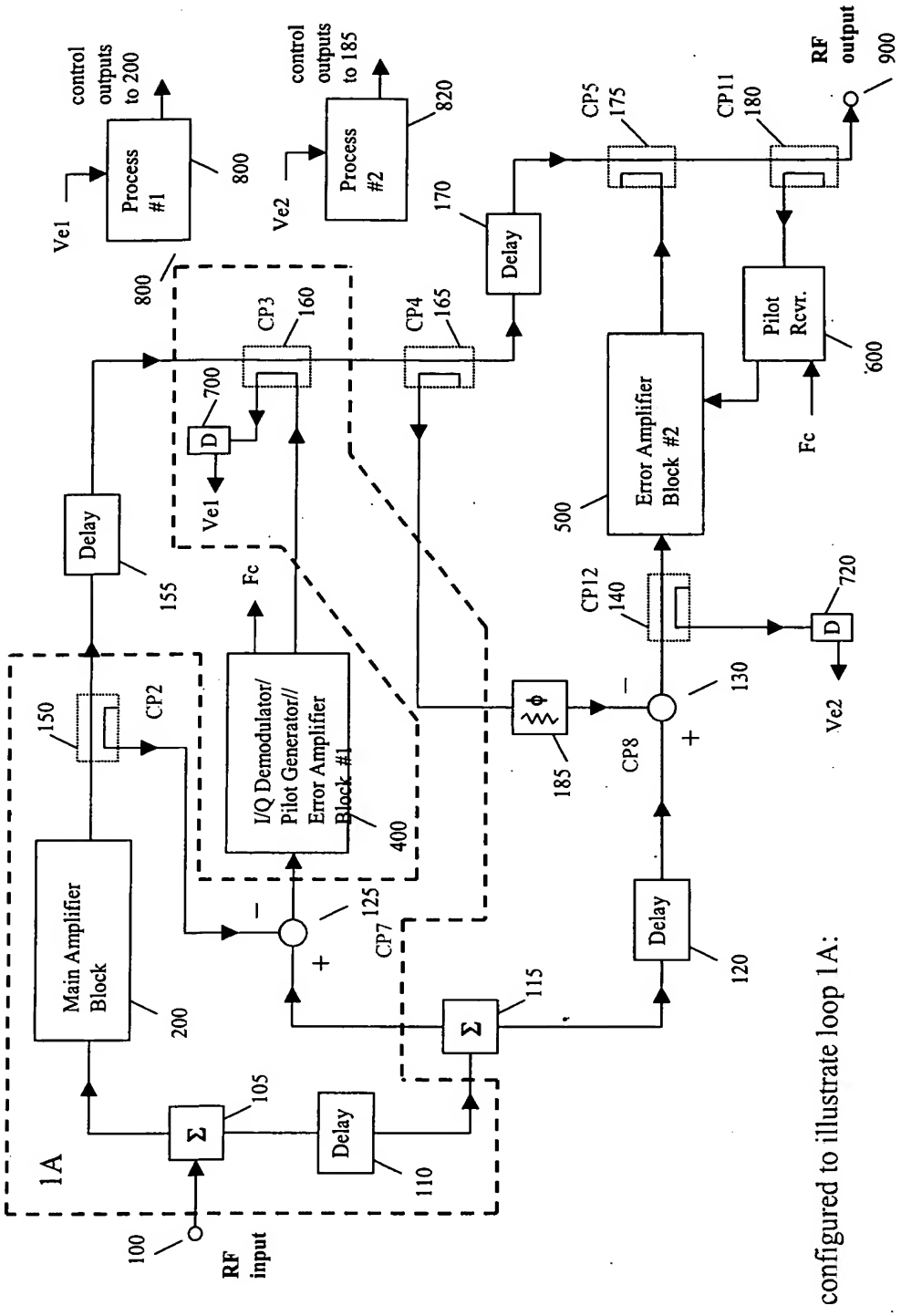
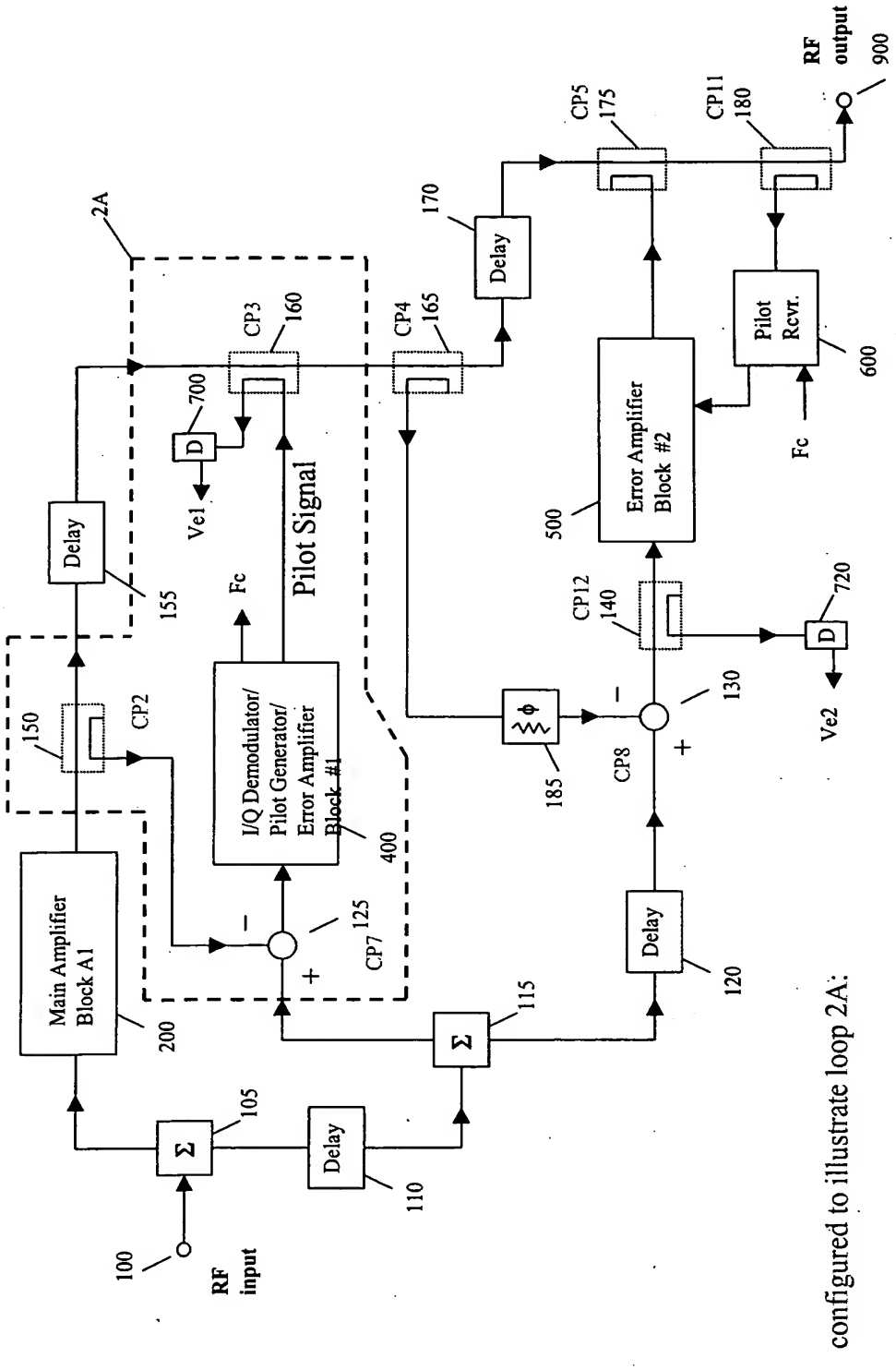
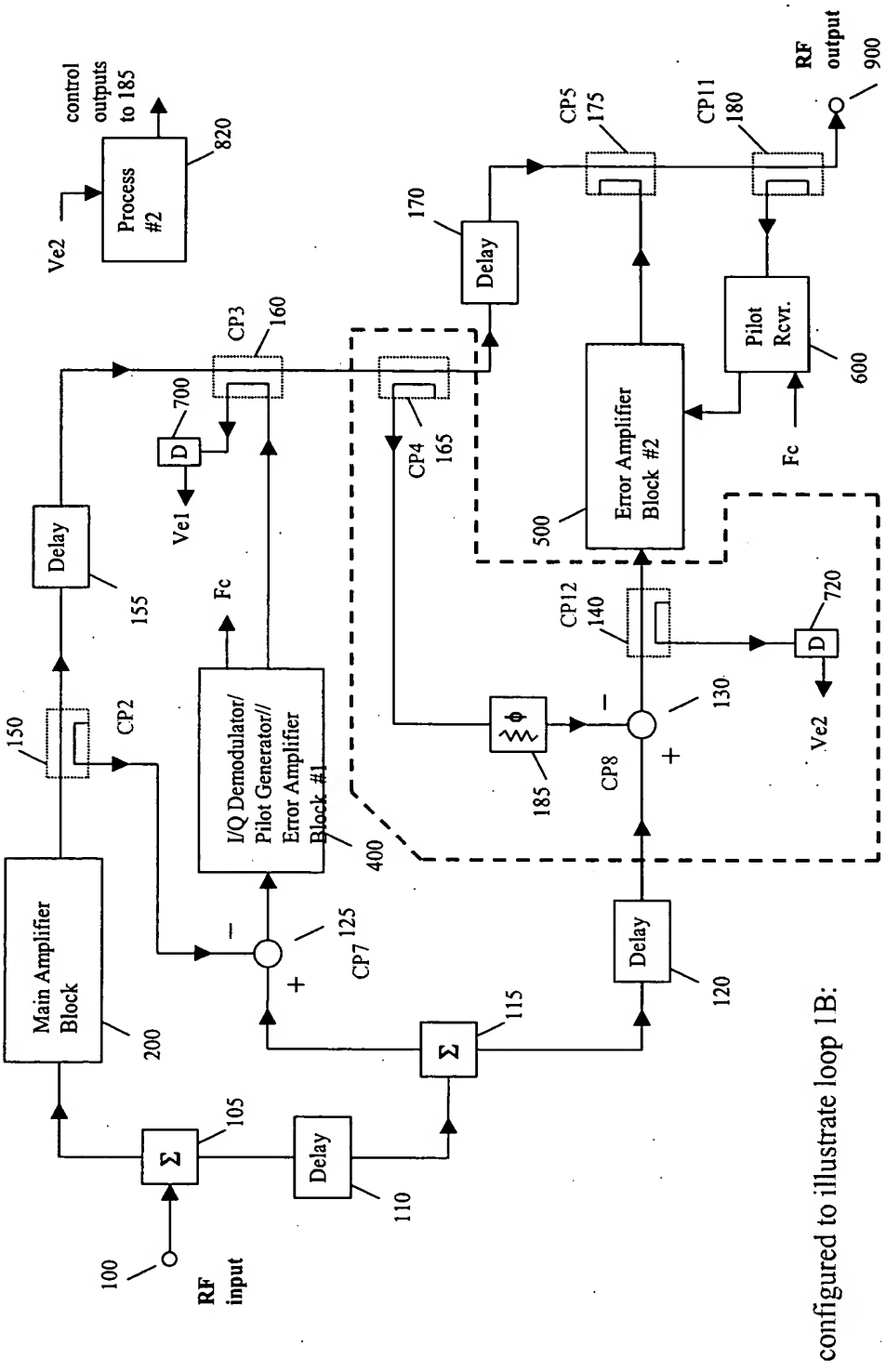

control outputs to 200
Process #1
800
Ve1
control outputs to 185
Process #2
820
Ve2
RF output
900
CP5
175
CP11
180
170
Delay
800
CP3
160
CP4
165
700
D
Ve1
Delay
155
Fc
I/Q Demodulator/ Pilot Generator// Error Amplifier Block #1
400
Error Amplifier Block #2
500
Pilot Rcvr.
600
Fc
CP12
140
720
D
Ve2
150
CP2
130
185
CP8
Main Amplifier Block
200
125
CP7
115
Σ
Delay
120
105
Σ
Delay
110
1A
100
RF input
configured to illustrate loop 1A:

FIG. 4



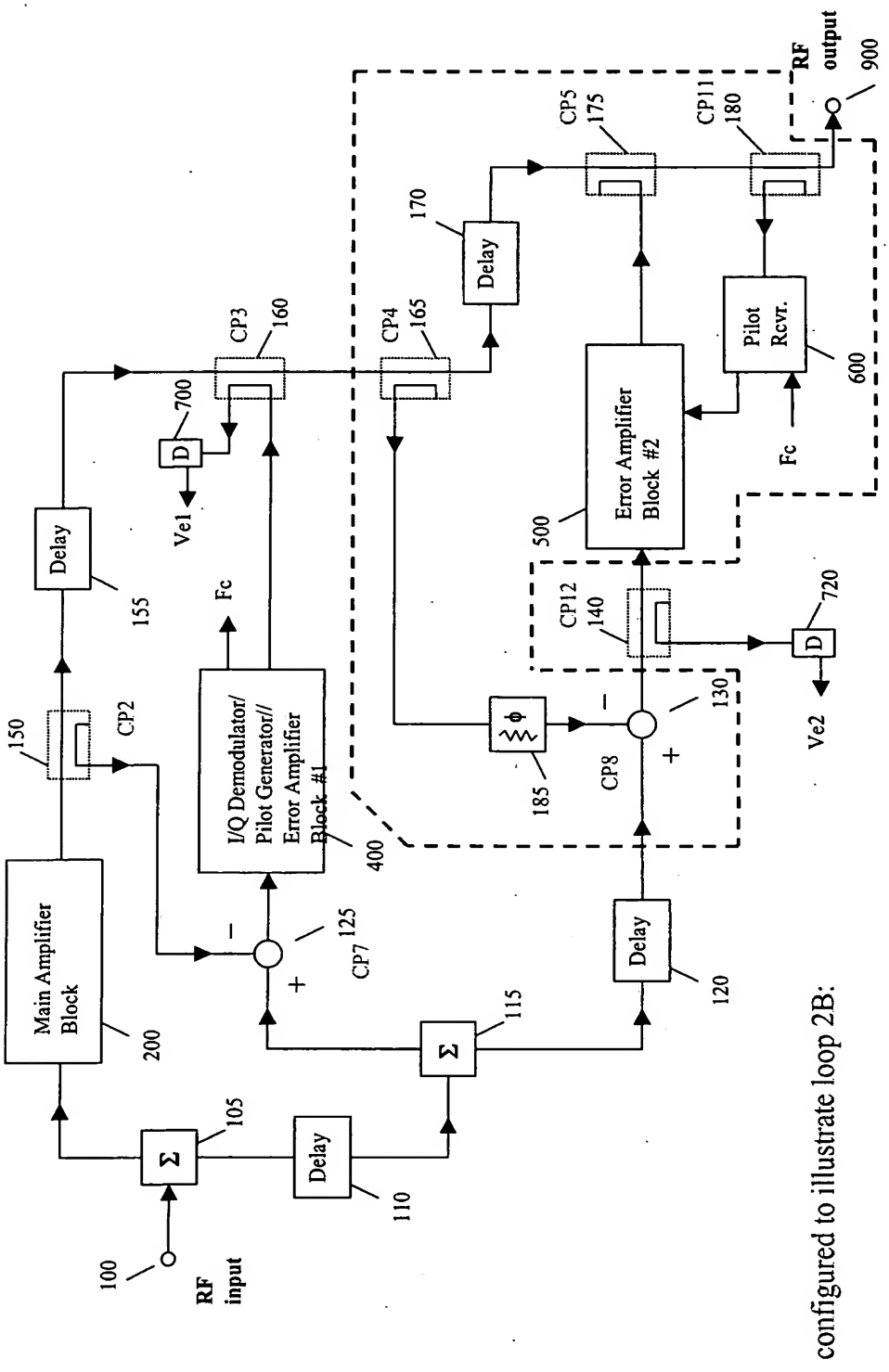
configured to illustrate loop 2A:

FIG. 5



configured to illustrate loop 1B:

FIG. 6



configured to illustrate loop 2B:

FIG. 7

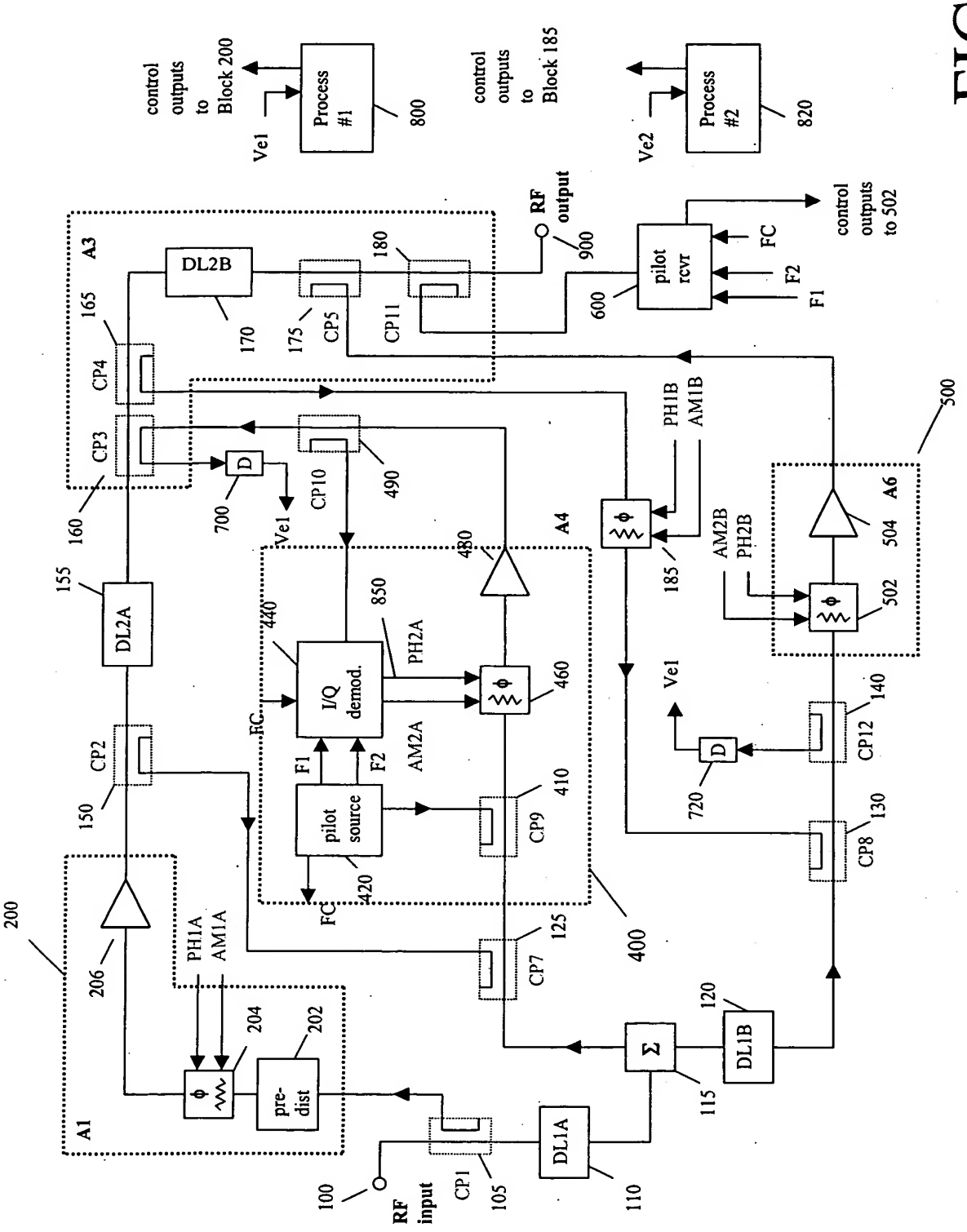

control outputs to Block 200
Process #1
800
Ve1
control outputs to Block 185
Process #2
820
Ve2
RF output
900
pilot rcvr
600
FC
F2
F1
control outputs to 502
A3
DL2B
170
165
CP4
CP3
160
175
CP5
CP11
180
700
D
Ve1
CP10
490
480
A4
PH1B
AM1B
500
A6
504
AM2B
PH2B
185
502
155
DL2A
440
I/Q demod.
850
PH2A
460
FC
F1
F2
AM2A
CP2
150
pilot source
420
410
CP9
FC
Ve1
720
D
140
CP12
130
CP8
200
206
PH1A
AM1A
125
CP7
400
204
202
pre-dist
A1
120
DL1B
Σ
115
100
RF input
CP1
105
DL1A
110

FIG. 8

FIG. 9

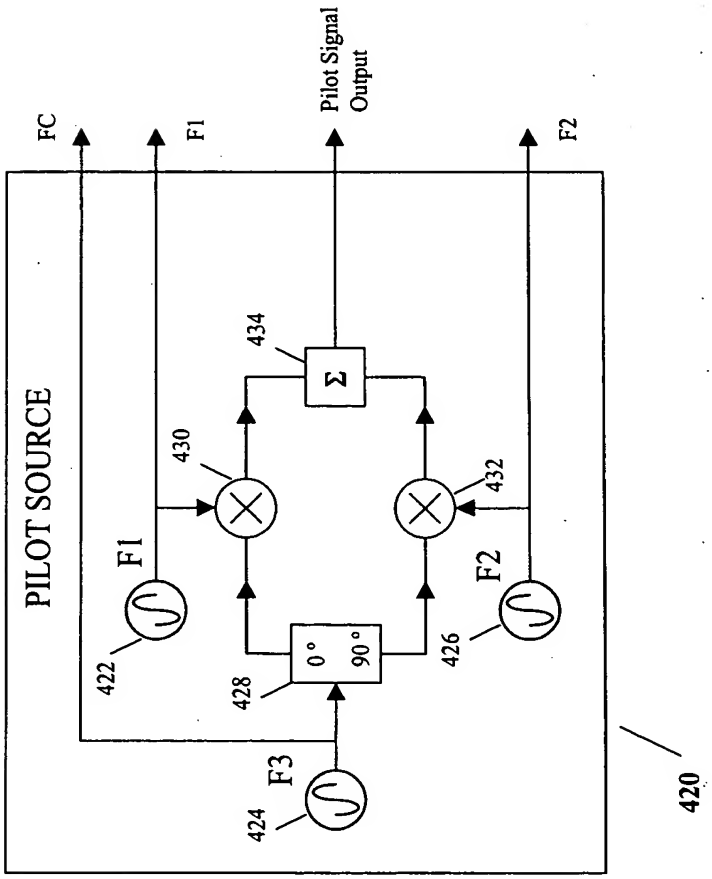

FC
F1
Pilot Signal Output
F2
PILOT SOURCE
434
Σ
430
432
F1
F2
422
428
0°
90°
426
F3
424
420

FIG. 10

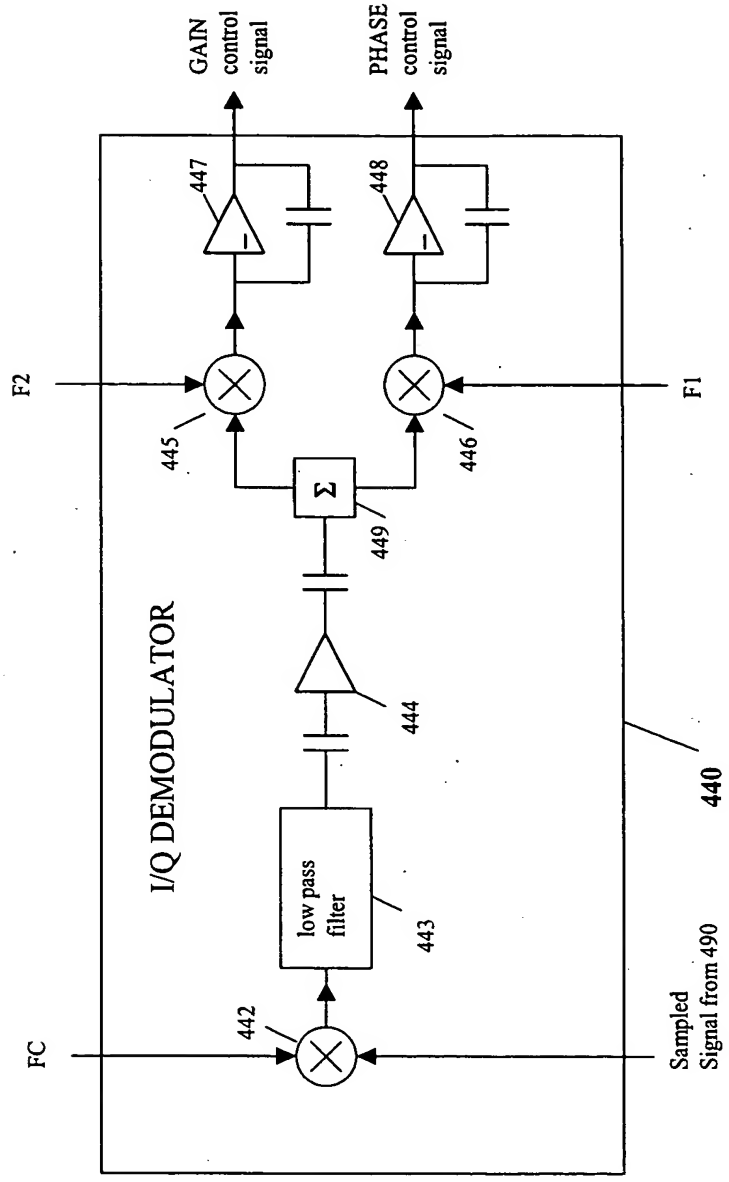

GAIN control signal
PHASE control signal
447
448
F2
F1
445
446
Σ
449
I/Q DEMODULATOR
444
low pass filter
443
440
442
FC
Sampled Signal from 490

FIG. 11

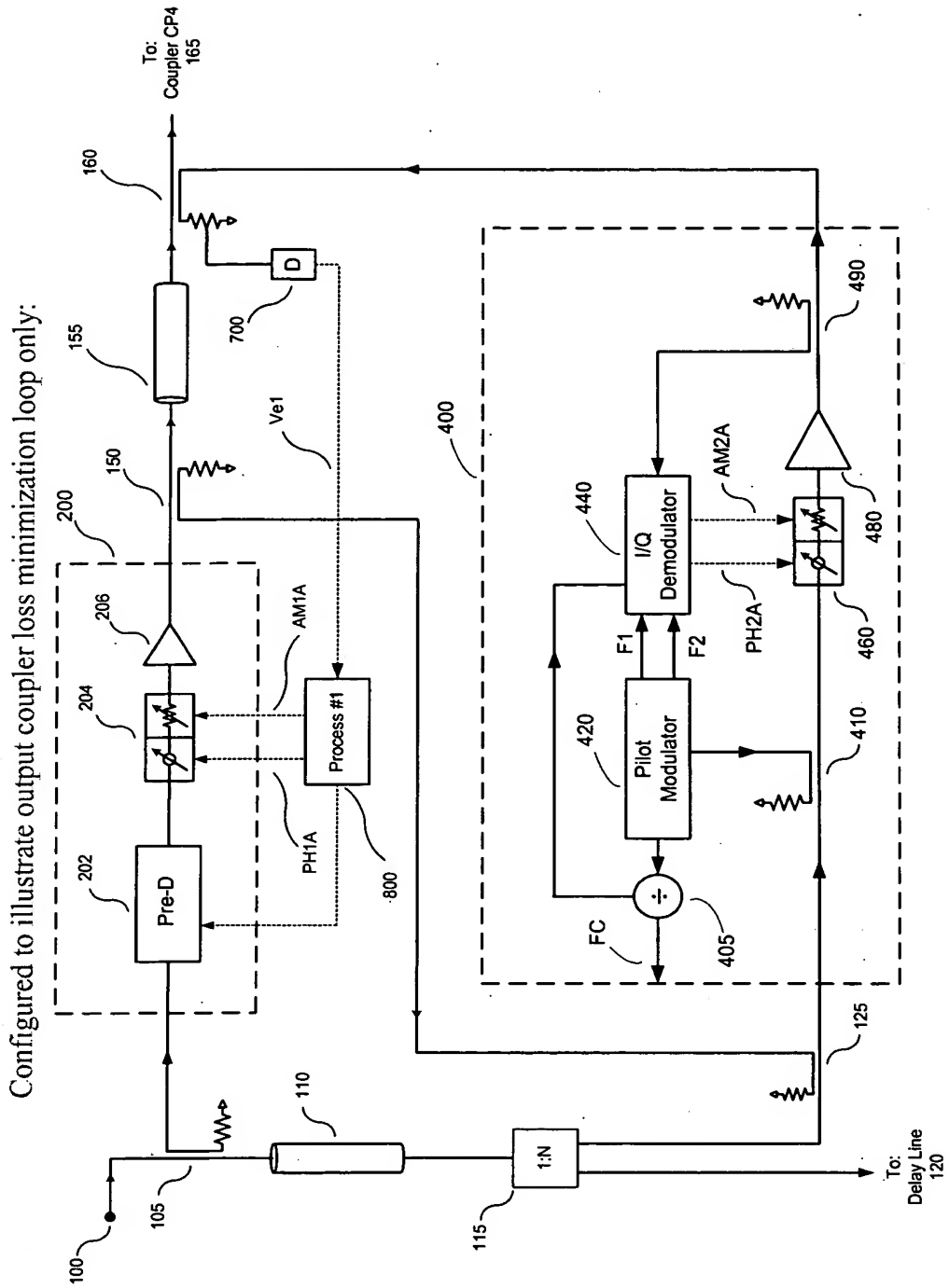
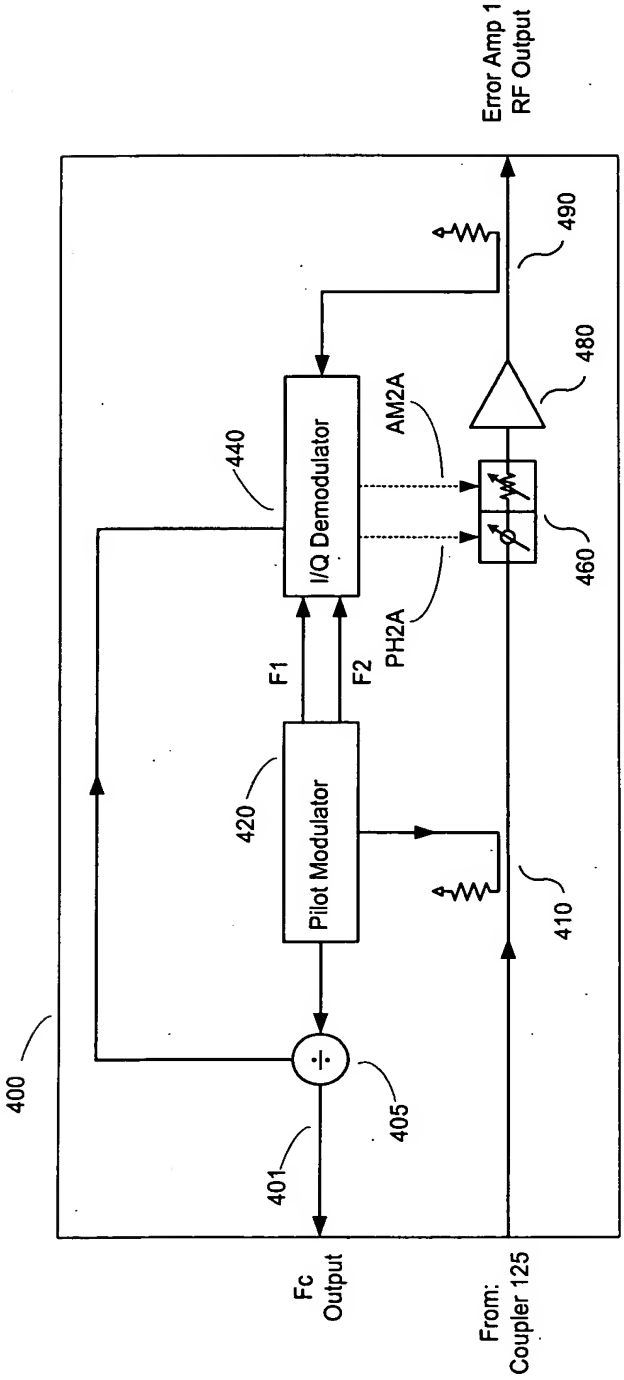

Configured to illustrate output coupler loss minimization loop only:
To: Coupler CP4 165
160
155
700
D
Ve1
150
200
206
AM1A
204
Process #1
202
Pre-D
PH1A
800
400
490
AM2A
440
I/Q Demodulator
480
F1
F2
PH2A
460
420
Pilot Modulator
410
FC
405
125
110
1:N
To: Delay Line 120
105
115
100

FIG. 12


Error Amp 1
RF Output
490
480
AM2A
440
I/Q Demodulator
460
PH2A
F1
F2
420
Pilot Modulator
410
400
405
401
Fc
Output
From:
Coupler 125

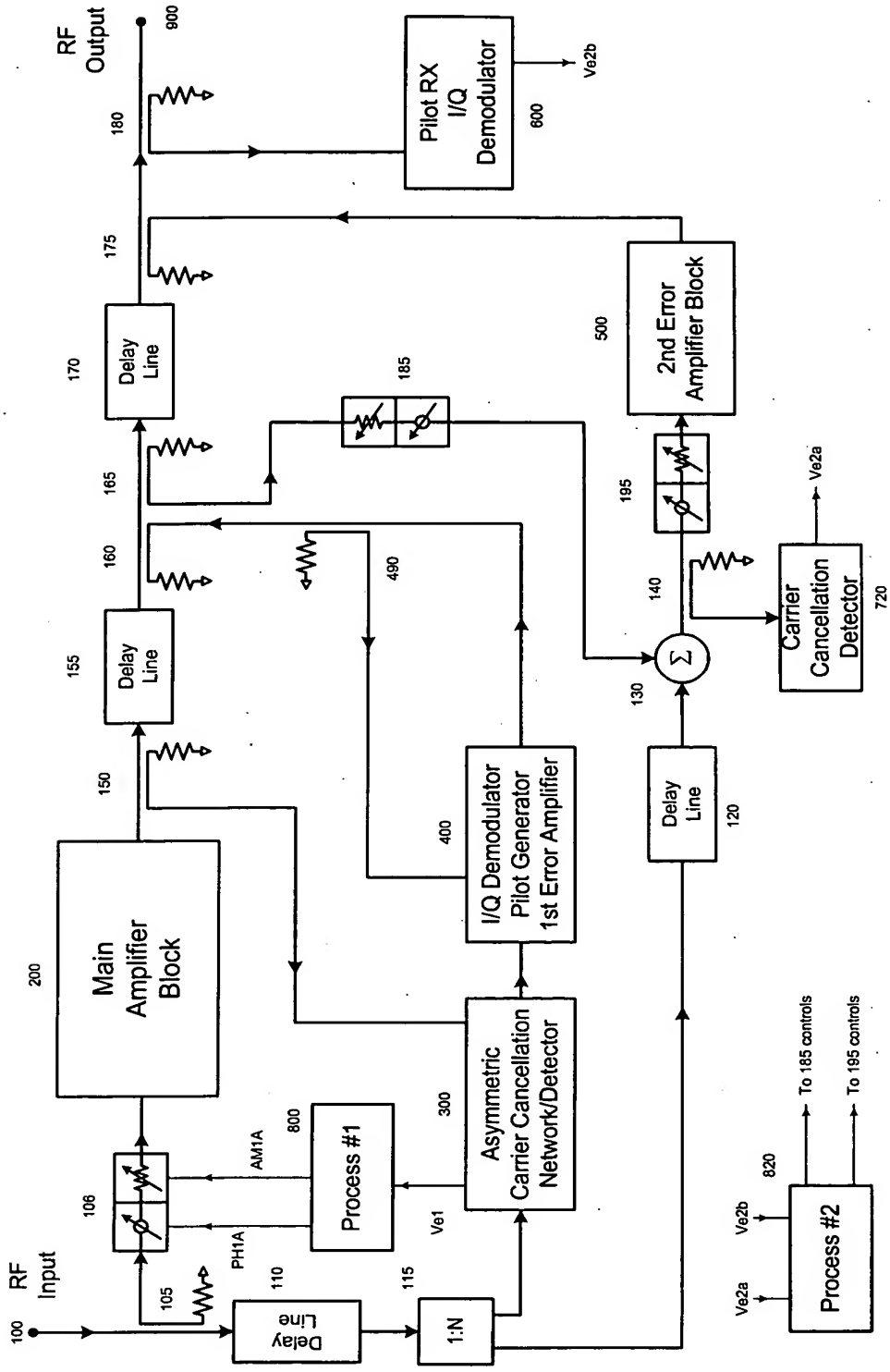

RF Input
100
105
106
110
Delay Line
115
1:N
PH1A
AM1A
800
Process #1
Ve1
300
Asymmetric Carrier Cancellation Network/Detector
200
Main Amplifier Block
150
Delay Line
155
160
Delay Line
165
170
Delay Line
175
180
RF Output
900
400
I/Q Demodulator Pilot Generator 1st Error Amplifier
490
120
Delay Line
130
Σ
140
195
185
500
2nd Error Amplifier Block
Pilot RX I/Q Demodulator
600
Ve2b
Ve2a
720
Carrier Cancellation Detector
Ve2a
Ve2b
820
Process #2
To 185 controls
To 195 controls

FIG. 13A

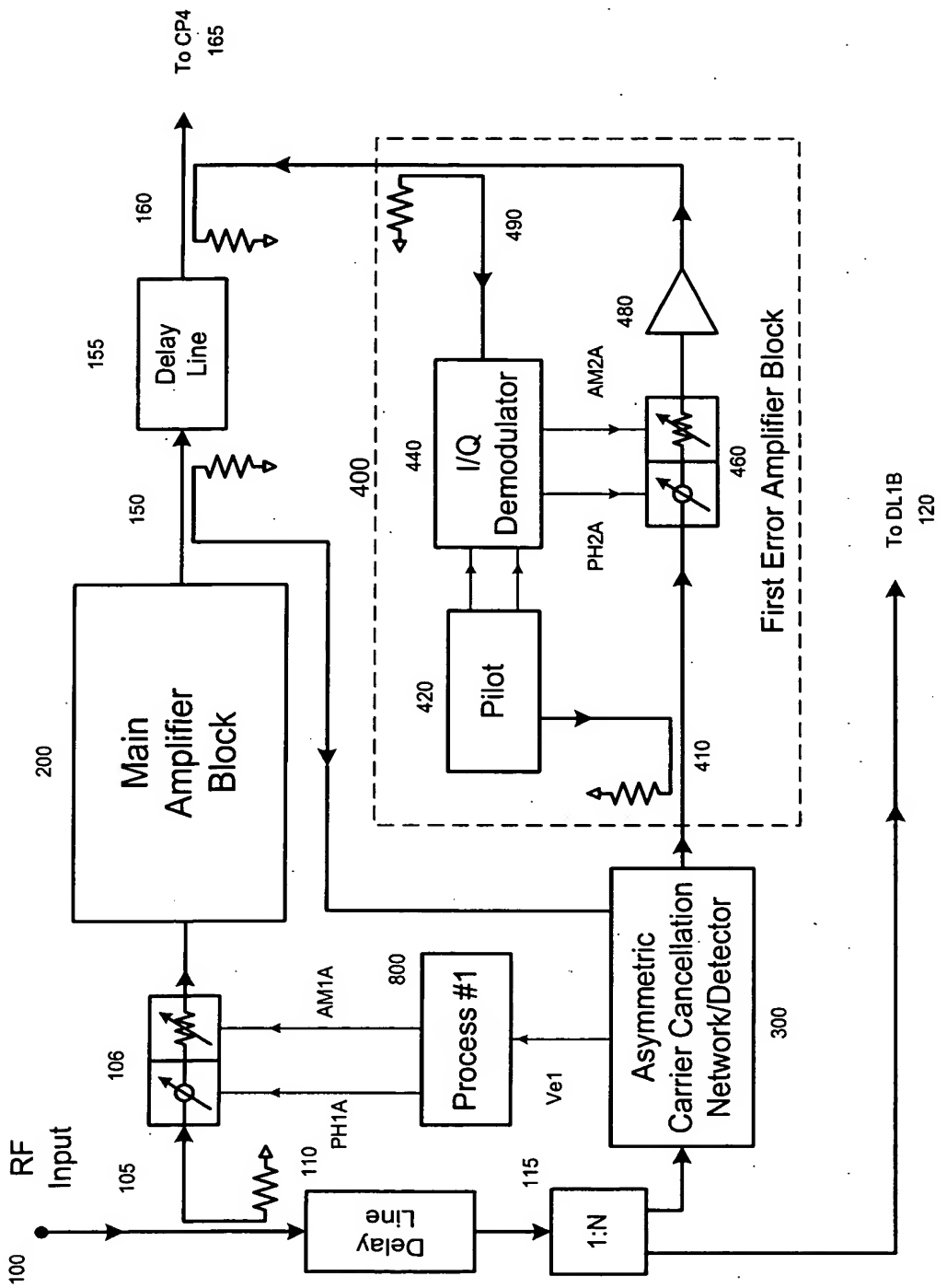
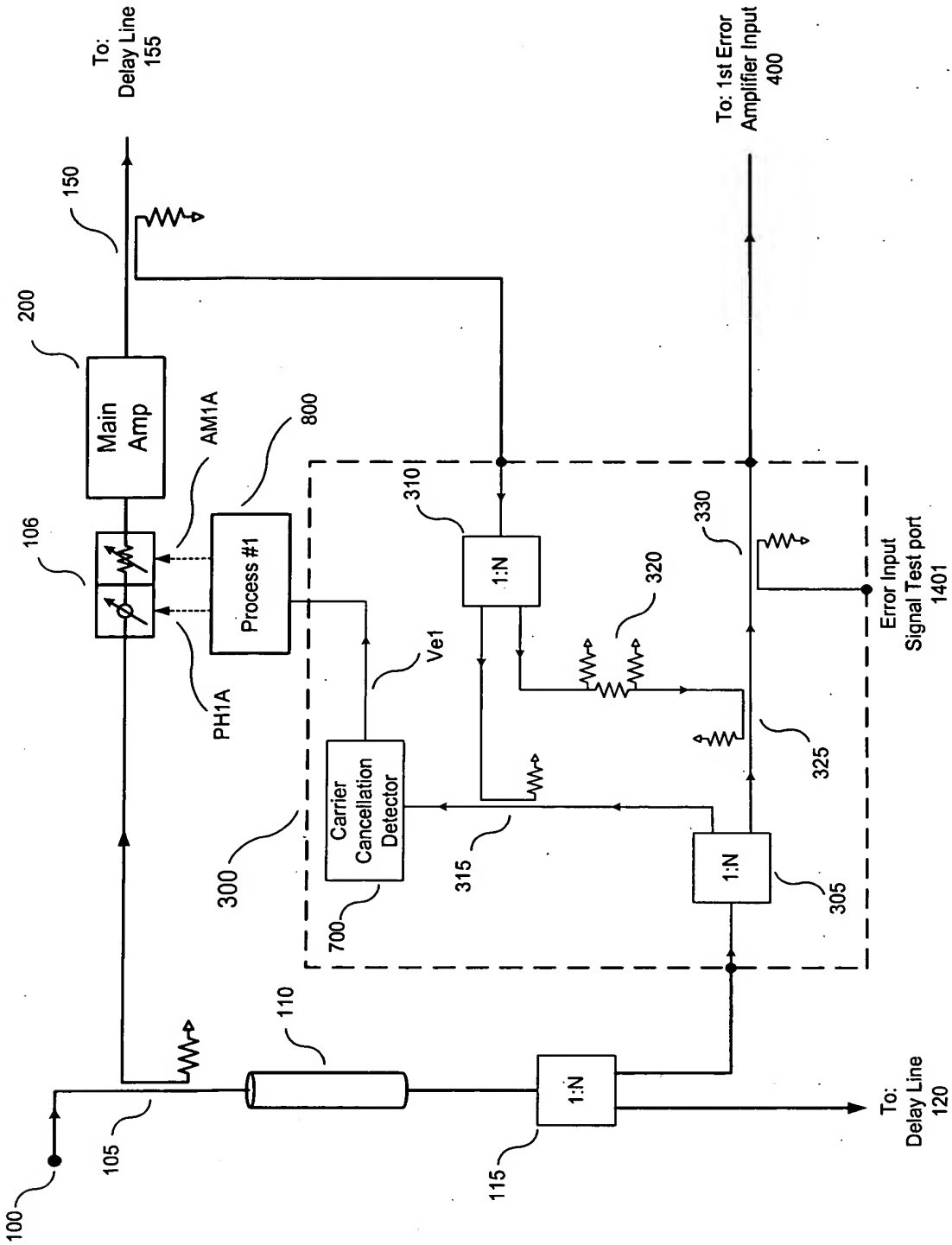

To CP4
165
160
155
Delay Line
150
200
Main Amplifier Block
400
440
I/Q Demodulator
490
480
AM2A
PH2A
460
420
Pilot
410
First Error Amplifier Block
To DL1B
120
106
AM1A
PH1A
800
Process #1
Ve1
Asymmetric Carrier Cancellation Network/Detector
300
RF Input
100
105
110
Delay Line
115
1:N

FIG. 13B

FIG. 14


To: Delay Line 155
To: 1st Error Amplifier Input 400
150
200
Main Amp
AM1A
800
106
Process #1
PH1A
310
1:N
330
320
Error Input Signal Test port 1401
Ve1
325
Carrier Cancellation Detector
300
315
700
1:N
305
110
1:N
To: Delay Line 120
105
115
100

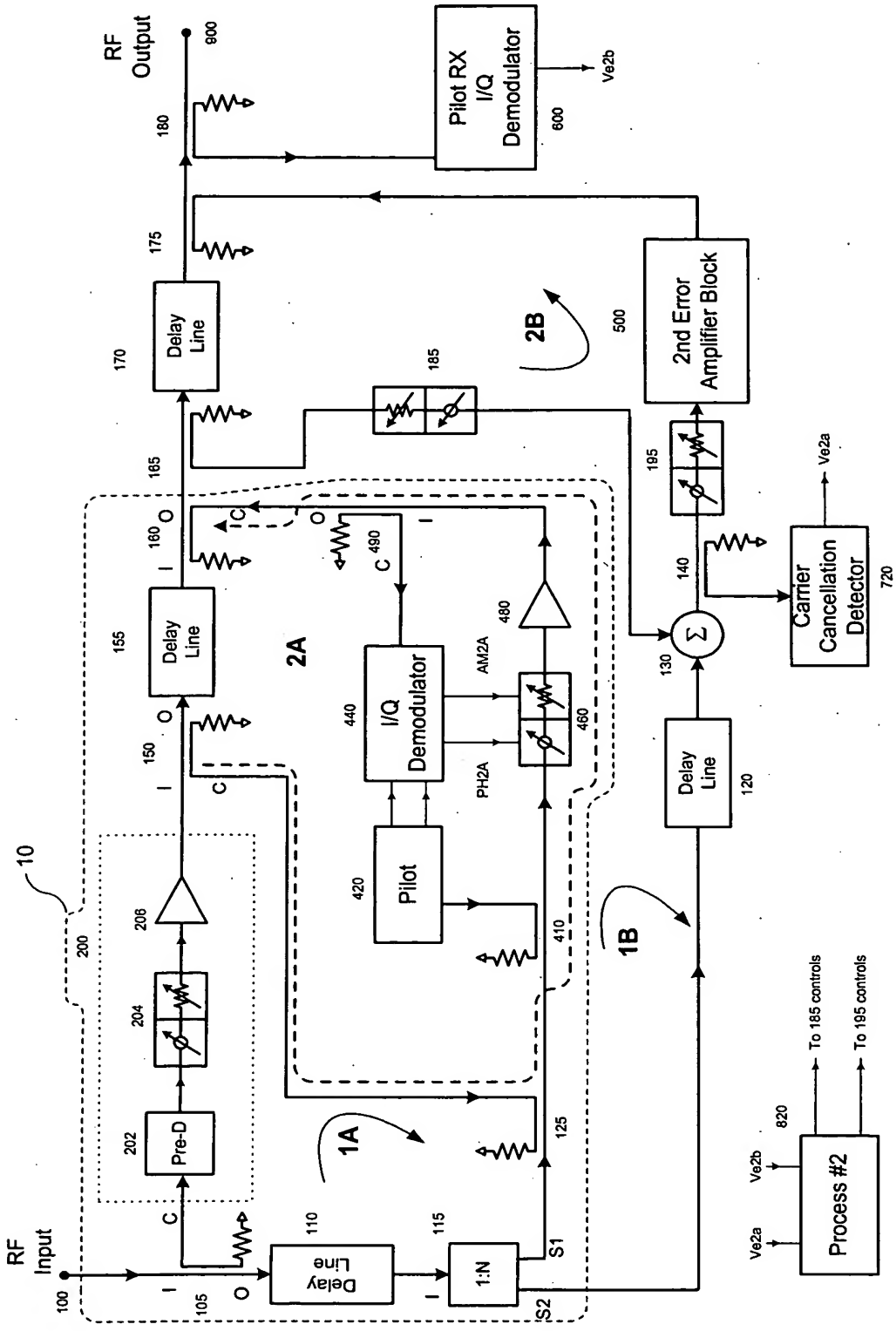

1st Error Amplifier Stabilization
RF Input
RF Output
Pilot RX I/Q Demodulator
Ve2b
2nd Error Amplifier Block
Carrier Cancellation Detector
Ve2a
Delay Line
Pre-D
I/Q Demodulator
Pilot
1:N
Process #2
To 185 controls
To 195 controls
1A
1B
2A
2B
AM2A
PH2A
S1
S2

FIG. 15

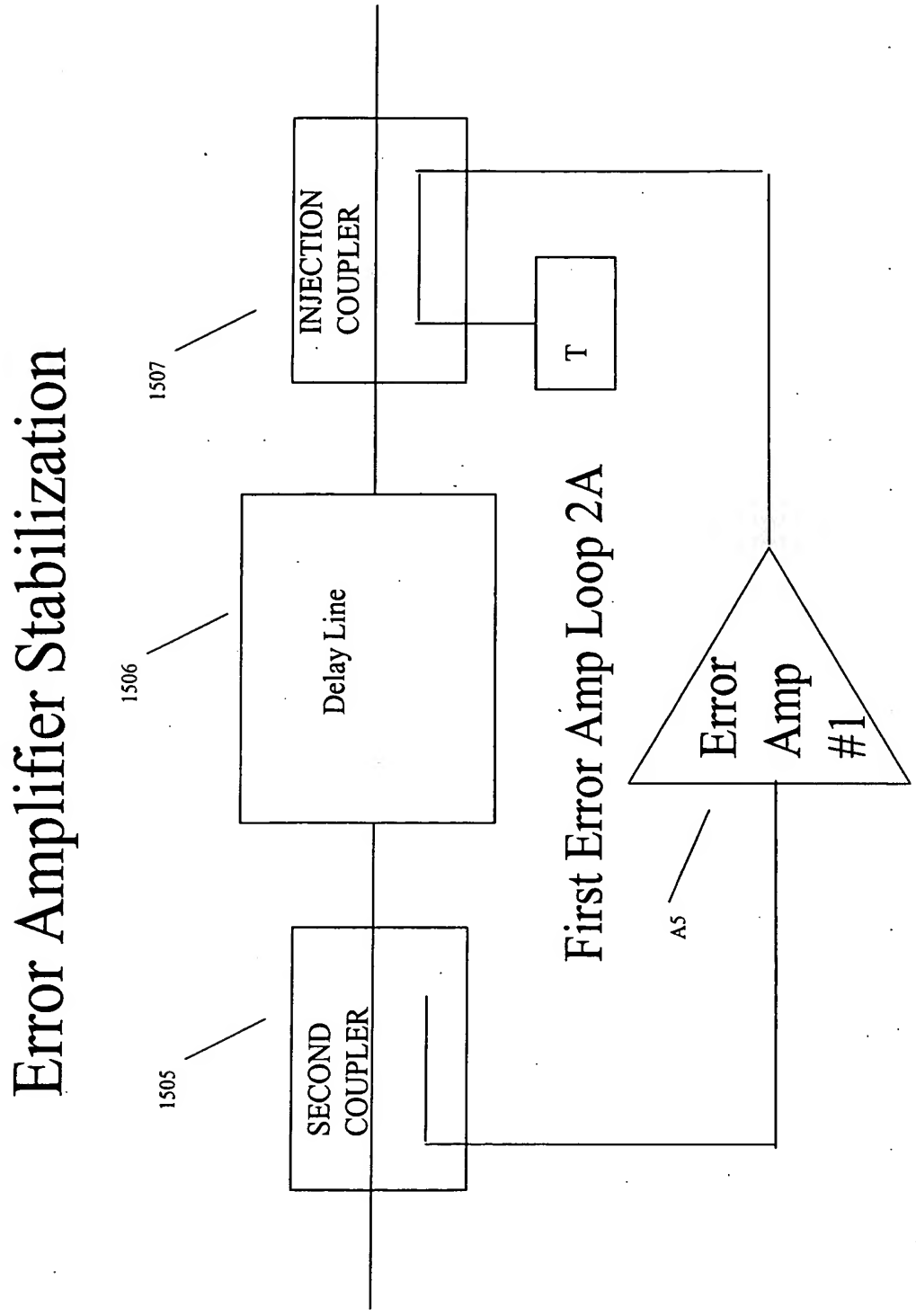
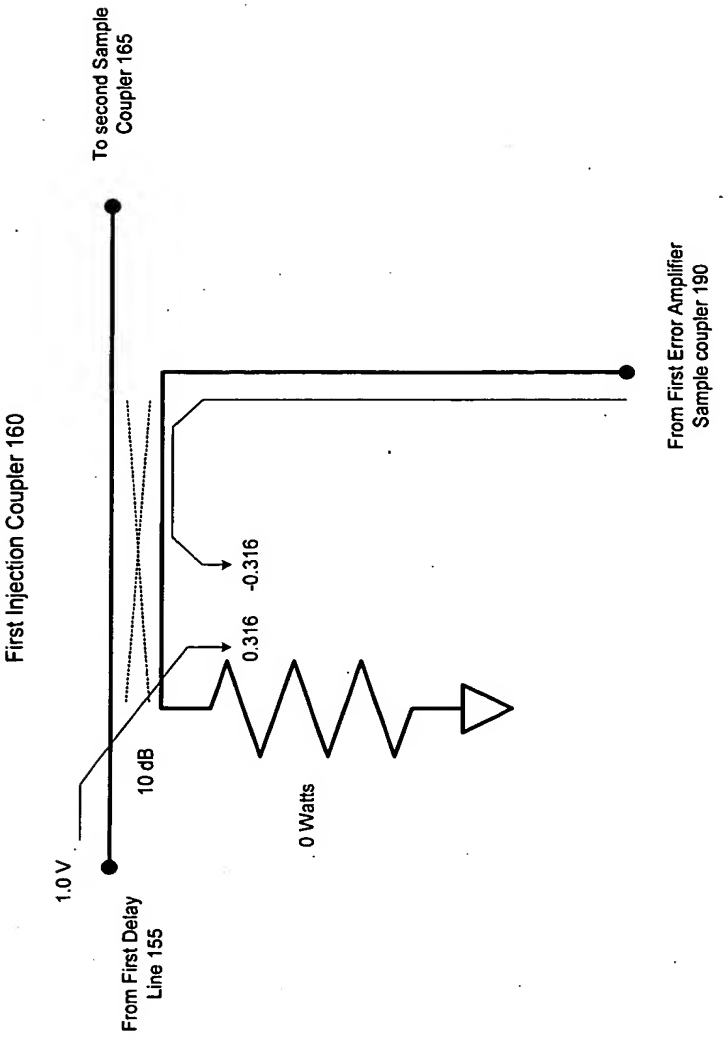

Error Amplifier Stabilization
1507
INJECTION COUPLER
T
1506
Delay Line
First Error Amp Loop 2A
Error Amp #1
A5
1505
SECOND COUPLER

FIG. 16

FIG. 17


To second Sample Coupler 165
From First Error Amplifier Sample coupler 190
First Injection Coupler 160
-0.316
0.316
10 dB
0 Watts
1.0 V
From First Delay Line 155

Carrier Re-Injection

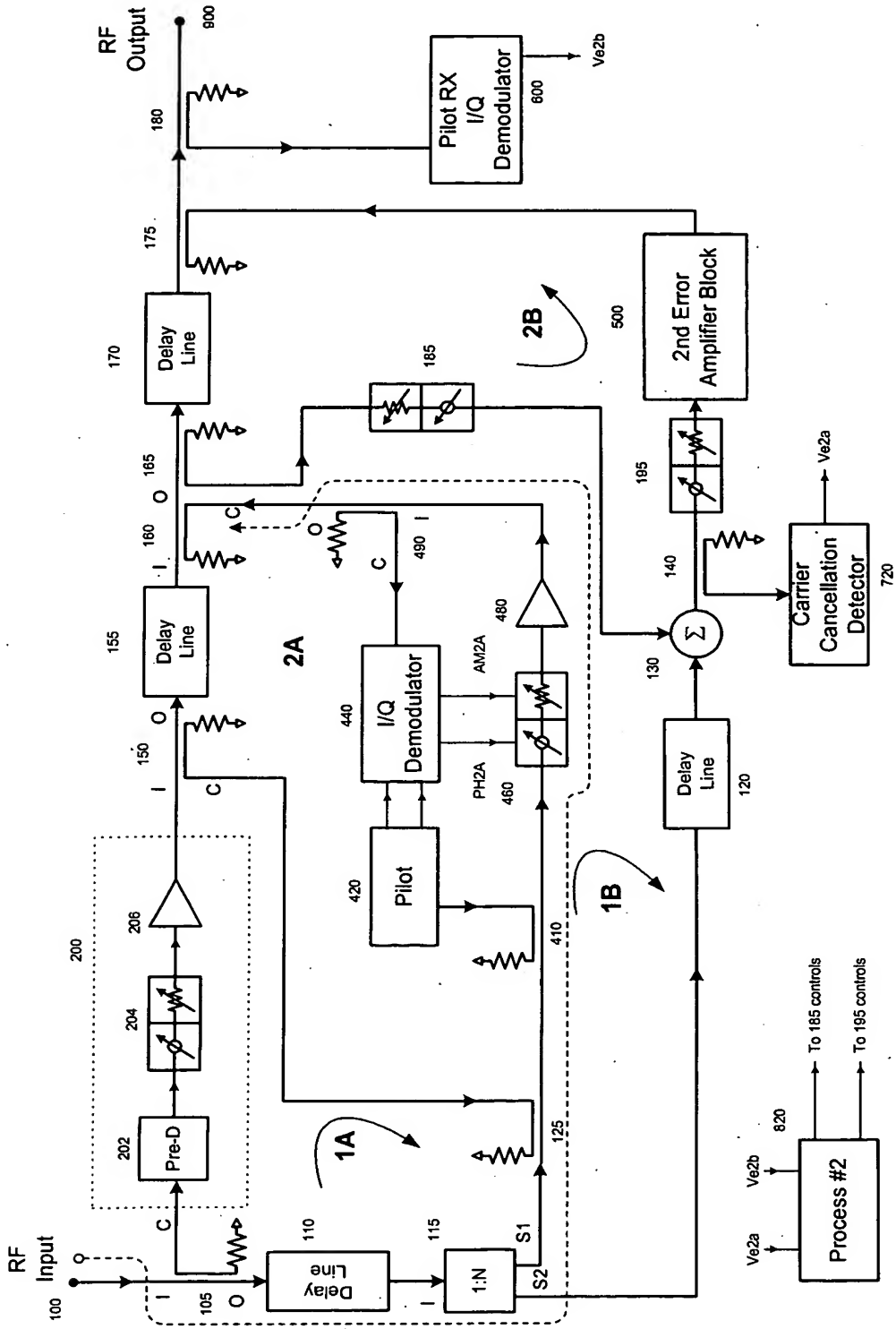


FIG. 18

Non-Overlapping Loop Adjustment

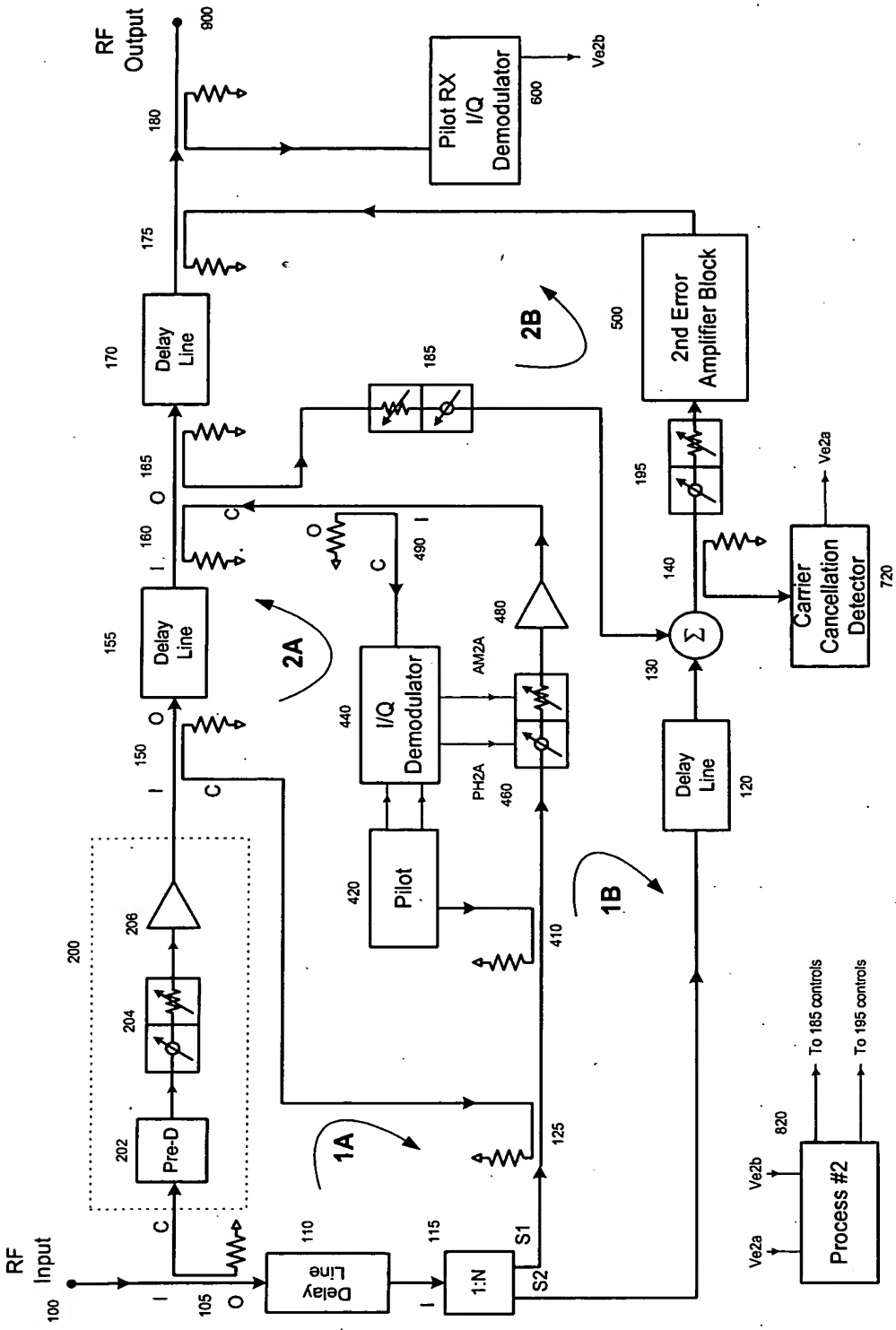


FIG. 19